I. PENDING CLAIMS

1. (Previously Presented) An integrated circuit comprising:
   a semiconductor substrate;
   a buried insulation layer directly over the semiconductor substrate;
   a semiconductor mesa over the buried insulation layer; and,
   a guard ring substantially surrounding the semiconductor mesa, wherein the guard ring extends through the buried insulation layer contacting the semiconductor substrate, and wherein the guard ring is arranged to provide RF isolation for the semiconductor mesa.

2. (Original) The integrated circuit of claim 1 wherein the semiconductor substrate comprises a high resistivity semiconductor substrate.

3. (Original) The integrated circuit of claim 1 wherein the semiconductor substrate comprises a silicon substrate, wherein the buried insulating layer comprises a buried silicon oxide layer, and wherein the semiconductor mesa comprises a silicon mesa.

4. (Original) The integrated circuit of claim 3 wherein the silicon substrate comprises a high resisitivity silicon substrate.

5. (Original) The integrated circuit of claim 1 wherein the semiconductor substrate is doped in an area that is contacted by the guard ring.

6. (Original) The integrated circuit of claim 5 wherein the semiconductor substrate comprises a high resitivity semiconductor substrate.

7. (Original) The integrated circuit of claim 5 wherein the semiconductor substrate comprises a silicon substrate, wherein the buried insulating layer comprises a buried silicon oxide layer, and wherein the semiconductor mesa comprises a silicon mesa.

8. (Original) The integrated circuit of claim 7 wherein the silicon substrate comprises a high resisitivity silicon substrate.

9. (Original) The integrated circuit of claim 1 further comprising an insulating ring between the guard ring and the semiconductor mesa, wherein the insulating ring surrounds the semiconductor mesa.

10. (Original) The integrated circuit of claim 9 wherein the semiconductor substrate comprises a high resistivity semiconductor substrate.

11. (Original) The integrated circuit of claim 9 wherein the semiconductor substrate comprises a silicon substrate, wherein the buried insulating layer comprises a buried silicon oxide layer, wherein the insulating ring comprises a silicon oxide insulating ring, and wherein the semiconductor mesa comprises a silicon mesa.

12. (Original) The integrated circuit of claim 11 wherein the silicon substrate comprises a high resistivity silicon substrate.

13. (Original) The integrated circuit of claim 9 wherein the semiconductor substrate is doped in an area that is contacted by the guard ring.

14. (Original) The integrated circuit of claim 13 wherein the semiconductor substrate comprises a high resistivity semiconductor substrate.

15. (Original) The integrated circuit of claim 13 wherein the semiconductor substrate comprises a silicon substrate, wherein the buried insulating layer comprises a buried silicon oxide layer, wherein the insulating ring comprises a silicon oxide insulating ring, and wherein the semiconductor mesa comprises a silicon mesa.

16. (Original) The integrated circuit of claim 15 wherein the silicon substrate comprises a high resistivity silicon substrate.

17. (Original) The integrated circuit of claim 1 wherein the guard ring comprises a low resistivity guard ring.

18. (Original) The integrated circuit of claim 1 wherein the guard ring comprises a metal guard ring.

19. (Original) The integrated circuit of claim 18 wherein the metal guard ring comprises a tungsten guard ring.

20-39. (Withdrawn)